International Journal of Scientific & Engineering Research, Volume 4, Issue 8, August 2013
ISSN 2229-5518

Assymetrical full bridge converter for photovoltaic systems

Prabin James,Teena jacob

Abstract— This paper describes a step-up DC-DC converter, which main task is to increase the voltage from a low level drawn from a photovoltaic (PV) panel, to a high controlled level for a connected inverter. Photovoltanic cell operated with a maximum power point tracking technique.The converter also provides an electrical isolation of PV panels from the grid. In the DC-DC converter asymmetrical full bridge converter topology is used. The converter operates at high switching frequency to achieve small size of the power transformer. The main benefit of this converter is zero-voltage switching (ZVS) of primary MOSFETs and zero-current switching (ZCS) of rectifier diodes over the entire operating range. Advantage of used topology is that the converter can be controlled by a simple 8bit microcontroller (MCU). A simulated model with maximum efficiency was built to verify properties of the asssymetrical full bridge converter DC-DC converter.
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Index Terms— DC–DC converter, high-voltage gain, soft switching, zero-voltage switching (ZVS), zero-current switching (ZCS)..

1. INTRODUCTION

In nowadays the consumption of fossil fuels is on its maximum level, and new sources of oil or gas are discovered only rarely. And therefore we must think how we will compensate this deficit. One of options is using renewable power sources. Today the power of water and wind are most used. However with increasing development in photovoltaics the solar energy is more and more used nowadays. This increase is related to increasing efficiency of transformation of solar energy to electrical energy. Now, the common efficiency of PV cells is over 15 %, and in the laboratory was achieved efficiency up to 42 %. Rising demand on a market for photovoltaic is related to reducing cost of PV panels and benefits which many countries offer.

For using the energy drawn from PV panels, we need special type of a converter. The type of the converter depends on method how we use PV panels. If system of PV panels and converter is not connected to power grid, we talk about off-grid system. At no-load, the energy obtained from PV panels is usually stored in batteries. If the consumption of energy begins, the converter starts to transfer the energy to the load through the inverter. If the level of power obtained from PV panels is higher than the system can offer, the converter starts to draw the energy from batteries.Photovoltaic systems connected to an electric grid, called on-grid, are more often used today. In this case special inverters are used, which convert the energy fromPV panels directly into the grid.It is desired to use the renewable energy sources with maximum efficiency. One of the possibilities of the technique is increase the power of the inverter. There are quantities of inverters for PV systems on the market. Some inverters include DC-DC step-up converter, depending on whether the inverter is connected to the string of PV panels with voltage higher than the maximum value of the grid voltage.

- *Prabin James is currently pursuing masters degree program in Power electronics and drives in Calicut university,India, PH-+919446627278. E-mail: prabinjesus@mail.com*
- *Co-Author name is currently pursuing masters degree program in electric power engineering in University, India E-mail: teenajacob101@yahoo.co.in (This information is optional; change it according to your need.)*

2. PRINCIPLE OF OPERATION

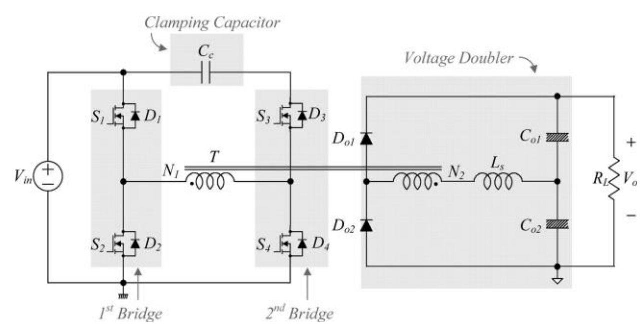

Fig 1:proposed converter system

fig fig1 shows a proposed model for asymmetrical full bridge converter with high-voltage gain.The asymmetrical pulse width modulation (APWM) technique is applied to the proposed converter to eliminate switching losses and maintain low conduction loss. The limitation of the maximum duty cycle disappears in the proposed topology. The proposed converter features high-voltage gain, fixed switching frequency, soft-switching operations of all power switches and output diodes, and clamped voltages across power switches and output diodes. The reverse recovery problem of the output diodes is significantly alleviated due to an additional inductor at the secondary side. Therefore, the proposed converter shows high efficiency and it is suitable for high-voltage applications The proposed converter has four power switches S1 through S4 . There is also the clamping capacitor Cc between top side switches S1 and S3 of two switch bridges. The voltages across the switches S1 and S2 in the first bridge are confined to the input voltage Vin . The clamping capacitor Cc can clamp the voltages across the switches S3 and S4 in the second bridge. The output stage of the proposed converter has a voltage doubler structure that consists of the secondary winding N2 of the transformer T, the serial inductor Ls , the output capacitors Co1 , and Co2 , and the output diodes Do1 and Do2 . According to the voltage doublers structure, the voltage gain increases and the voltage stresses of the output diodes are confined to the output voltage Vo without any auxiliary circuits. The equivalent circuit of the proposed converter is shown in Fig.3below

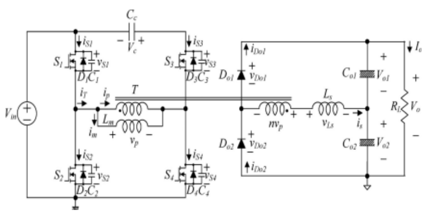

Fig 2.Equivalent circuit of the proposed converter

Its leakage inductance is included in the serial inductor Ls . To simplify the analysis, it is assumed that the clamping capacitor Cc has a large value and the voltage across Cc is constant as Vc under a steady state. Similarly, the output capacitor voltages are assumed to be constant as Vo1 and Vo2 , respectively.. The switch S1 (S4) and the switchS2 (S3) are operated asymmetrically and the duty cycle D is based on the switch S1 (S4). A small delay between driving signals for S1(S4) and S2 (S3) is a dead time for the switches. It prevents cross conduction and allows ZVS.

3.

4. MODES OF OPERATION

The operation of the proposed converter during a switching period Ts is divided into four modes. Before t0 ,the switches S2 and S3, and the output diode Do1 are conducting. At t0, the magnetizing current im and the secondary current is arrive at their minimum values Im2 and −IDo1, respectively.

4.1 MODE 1 [T0, T1]:

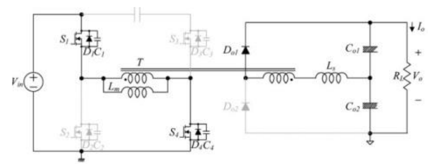

Fig 5 Mode 1

At t0, the switches S2 and S3 are turned OFF. Then, the energy stored in the magnetic components starts to charge/discharge the parasitic capacitances C1 through C4. Therefore, the voltages vS2 and vS3 start to rise from zero.

Similarly, the voltage vS4 starts to fall from Vin + Vc and the voltage vS1 starts to fall from Vin . Since all the parasitic output capacitances C1 through C4 are very small, this transition time interval is very short and it is ignored in Fig. 3.4 When the voltages vS1 and vS4 arrive at zero, their body diodes D1 and D4 are turned ON. Then, the gate signals are applied to the switches S1 and S4 . Since the currents have already flown through D1 and D4 and the voltages vS1 and vS4 are clamped as zero before the switches S1 and S4 are turned ON, zero-voltage turn-ON of S1 and S4 is achieved. With the turn-ON of S1 and S4, the primary voltage vp across Lm is Vin . Then, the magnetizing current im increases linearly from its minimum value Im2 as follows:

$$i_{m(t)} = i_{m(2)} - \frac{V_{in}}{L_m}(t - t_0)$$

Since the voltage vLs across Ls is nVin+Vo1 , the secondary current is increases from its minimum value −IDo1 as follows:

$$is(t) = -I_{Do1} + \frac{nVin + V_{o1}}{L_s}(t - t_0)$$

In this mode, the switch currents iS1 and iS4 can be written by

$$i_{s1(t)} = i_{s4(t)} = I_{m2} - nI_{do1} + (\frac{Vin}{Lm} + \frac{n(nVin + Vo1)}{Ls})(t - t_{o1})$$

4.2 MODE 2 [T1, T2]:

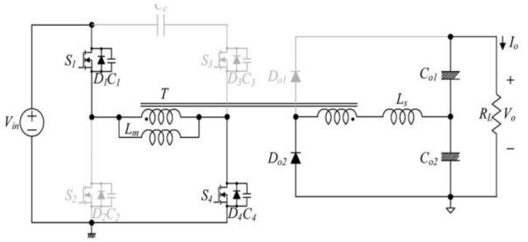

Fig 6 Mode 2

At t1 , the currents is and iDo1 arrive at zero and the diode Do1 is turned OFF. Then, the output diode Do2 is turned ON and its current increases linearly. Since the current changing rate of Do1 is controlled by the serial inductor Ls , its reverse-recovery problem is significantly alleviated. Since the voltage vls is (nVin−Vo2) in this mode, the current is are given by

$$i_s(t) = \frac{nV_{in} - V_{o2}}{L_s}(t - t_1)$$

Since the voltage vp is not changed in this mode. In this mode, the switch current iS1 and iS4 can be written by

$$i_{s1(t)} = i_{s4(t)} = I_m(t) + (\frac{Vin}{Lm} + \frac{n(nVin - V_{o2})}{Ls})(t - t_1)$$

4.3 MODE 3 [T2, T3]:

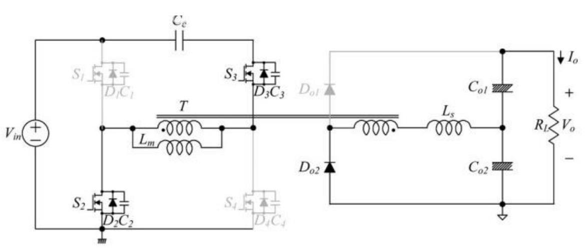

Fig 7 Mode 3

In this mode, the switches S1 and S4 are turned OFF at t2 . The parasitic capacitors C1 and C4 start to be charged from zero, whereas the parasitic capacitors C2 and C3 start to be discharged from Vin and Vin + Vc , respectively. With the same assumption as mode 1, this transition time interval is very short and it is ignored in Fig. 3.6 After the parasitic capacitors are fully charged and discharged, the voltages vS2 and vS3 become zero and the body diodes D2 and D3 are turned ON. Then, the gate signals are applied to the switches S2 and S3 . Since the currents have already flown through D2 and D3 and the voltages vS2 and vS3 are clamped as zero, zero-voltage turn-ON of S2 and S3 is achieved. With the turn-ON of S2 and S3, the voltage vp across Lm is −(Vin+Vc). Then, the current im decreases linearly from its maximum value Im1 as follows:

$$i_{m(t)} = I_{m1} - \frac{V_{in} + V_c}{L_s}(t - t_2)$$

Since the voltage vLs across Ls is −(n(Vin + Vc) +Vo2), the current is decreases from its maximum value IDo2 as follows:

$$i_{s(t)} = I_{Do2} - \frac{n(V_{in} + V_c) + V_{02}}{L_s}(\text{t - t}_2)$$

In this mode, the switch currents iS2 and iS3 can be written by

$$i_{s2(t)} = i_{s3(t)} = -I_{m1} - I_{Do2}(\frac{(V_{in} + V_c)}{L_m} + \frac{n(n(V_{in} + V_c + V_{o2}}{L_s}$$

4.4. MODE 4 [T4, T5]:

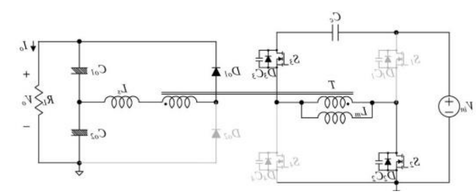

Fig8 :mode 4

In this mode, the currents is and iDo2 arrive at zero and the diode Do2 is turned OFF at t3. Then, the output diode Do1 is turned ON and its current increases linearly. Since the current changing rate of Do2 is controlled by Ls, its reverse-recovery problem is significantly alleviated. Since the voltage vLs is −(n(Vin + Vc)−Vo1), the current is is given by

Since the voltage vp is not changed in this mode. In this mode, the switch currents iS2 and iS3 can be written by

$$i_s(t) = -\frac{n(V_{in} + V_c) - V_{01}}{L_s}(t - t_3)$$

$$i_{s2}(t) = i_{s3}(t) = -i_m(t_3) + \left(\frac{(V_{in} + V_c)}{L_m} + \frac{n(n(V_{in} + V_c) - V_{o1}}{L_s}\right)(t - t_3)$$

At the end of this mode, the currents im and is arrive at Im2 and −IDo1 , respectively.

5. SIMULATION RESULTS

SPECIFICATION OF PROPOSED CONVERTER	
Input voltage	48V
Output voltage	367.4V

International Journal of Scientific & Engineering Research, Volume 4, Issue 8, August 2013
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Maximum output power Pomax	150W
Switching frequency fs	74 kHz
TS = 1/fs	13.5 µs
D	0.7
k	0.06

5.1 Input Voltage Waveform of Propsed Converter

In the simulation diagram an input voltage of 48V DC is applied.The resulting waveform shown below.Input pulse is measured by multimeter.

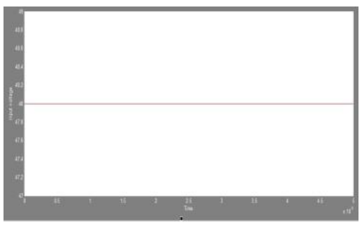

Fig 9 Input DC voltage waveform

5.2 ZVS Waveforms Of Power Switches

In the proposed converter system switches are zero voltage switched.In the simulation diagram double click the scope 8 and see ZVS waveform across the switches.

Simulation stop time=.005s
Sample time = 0.005e-5s

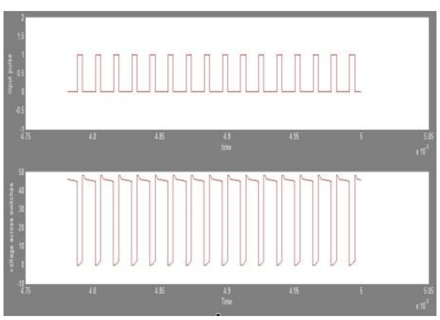

Fig 10 ZVS Matlab waveforms of the power switches

5.3 Output Voltage Waveform Of The Proposed Converter System

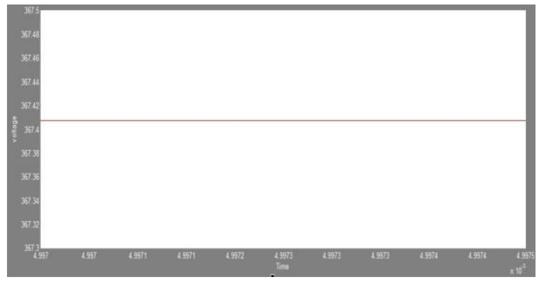

Fig 11 Output voltage of the proposed converter system

5.4 ZCS Waveforms Of output diodes

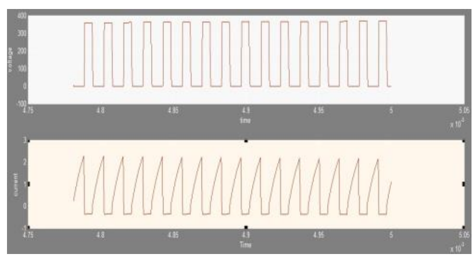

Fig 12 Zero current waveform across the diodes

When 48V is supplied to system older converter getting 4.1 voltage gain but 7.65 voltage gain getting new type of converter system.

6. Conclusion

In this paper, an asymmetrical full-bridge converter with high voltage gain has been presented. The ZVS of all power switches and ZCS of the output diodes are achieved. The proposed converter is able to provide a high efficiency and high-voltage gain with relatively low transformer turn ratio.Also, without any auxiliary circuits, the voltages across the switches and the output diodes are effectively clamped. Therefore, the proposed converter is suitable for high-voltage applications..

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Ist author

Prabin james got b-tech degree in N.S.S College of engineering palakkad.Now He was done M-tech in Power electronics and drives in Nehru college of engineering and research centre pampady Thrissur,Kerala.He was doing M-tech project on converter systems of solar.

2nd author

Teena jacob is M-tech in power electronics and Power systems.Now she is working it as a assistant professor in Nehru college of engineering and reaserch centre thrissur